* LT1054C is SOIC8 W not SOIC8
* Degenerate trace from C19
* C102 is on Backwards!!!!
* Input buffer EN should be PU not PD
* **VEE on CD4051BM should be -10V not +10V**
* Add PD resistors to UD / SEL lines of digital pot
* Leveling amplifier gain range should be shifted down about ½
* Replace negative feedback loop on peak detector with voltage offset
* Add test point to elliptic filter input and output
* REG103 pinout is wrong